SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2015-179130; filed on September 11, 2015; the entire contents of which are incorporated herein by reference.

FIELD

Embodiments described herein relate generally to a semiconductor device.

BACKGROUND

In a Schottky barrier diode (SBD) or a junction barrier Schottky diode (JBS) which is a type of the SBD, a PiN diode may be provided in an element region as a countermeasure against a forward surge current. By providing a PiN diode section in an element region, it is possible to make a large surge current flow using conductivity modulation of the PiN diode section.

In addition, in the SBD or the JBS, a termination structure is provided in a termination region in the periphery of an element region, in order to reduce the strength of an electric field in an end portion of the element region at the time of a reverse bias and prevent an element from being broken down.

It is preferable that a junction breakdown voltage of the element region is lower than that of the termination structure from a viewpoint of preventing an element breakdown at the time of reverse bias.

An example of related art includes JP-A-2013-115394.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic sectional view of a semiconductor device according to a first embodiment.

FIG. 2 is a schematic top view of the semiconductor device of the first embodiment.

FIG. 3 is a schematic sectional view of a semiconductor device according to a comparative form.

FIG. 4 is a schematic sectional view of a semiconductor device according to a second embodiment.

DETAILED DESCRIPTION

[0006]Exemplary embodiments provide a semiconductor device which can prevent element breakdown at the time of a reverse bias.

[0007]In general, according to one embodiment, a semiconductor device includes an element region which is a part a semiconductor layer including a first surface and a second surface; a termination region which is a part of the semiconductor layer and surrounds the element region; a first electrode which is provided on the first surface; a second electrode which is provided on the second surface; a first semiconductor region of a first conductive type which is provided in the semiconductor layer and a part of which comes into contact with the first electrode; a second semiconductor region of a second conductive type which is provided between the first semiconductor region in the element region and the first electrode; a third semiconductor region of the second conductive type which is provided between the second semiconductor region and the first electrode, is electrically coupled to the first electrode, and in which impurity concentration of the second conductive type is higher than impurity concentration of the second semiconductor region; and a fourth semiconductor region of the second conductive type which is provided between the first semiconductor region in the termination region and the first surface, is electrically coupled to the first electrode, and in which a distance between the fourth semiconductor region and the second surface is greater than a distance between the second surface and the second semiconductor region.

[0009]Hereinafter, exemplary embodiments will be descried with reference to the drawings. In the following description, the same symbols or reference numerals will be attached to the same members or the like, and description of the members or the like described once will be appropriately omitted.

[0010]In addition, in the following description, notation of n+, n and n-, and p+, p and p- represents relative levels of impurity concentrations of each conductive type. That is, it represents that n+-type impurity concentration is relatively higher than n-type impurity concentration, and n--type impurity concentration is relatively lower than n-type impurity concentration. In addition, it represents that p+-type impurity concentration is relatively higher than p-type impurity concentration, and p--type impurity concentration is relatively lower than p-type impurity concentration. There is a case in which n+ and n- are simply described as an n-type, and p+ and p- are simply described as a p-type.

[0011]Impurity concentration can be measured by, for example, a secondary ion mass spectrometry (SIMS). In addition, a relative level of the impurity concentration can also be determined from a level of carrier concentration which is obtained by, for example, a scanning capacitance microscopy (SCM). In addition, a distance of a depth of the like of an impurity region can be obtained by, for example, a SIMS. In addition, the distance of the depth of the like of the impurity region can be obtained from a synthetic image of, for example, a SCM image and an atomic force microscope (AFM) image.

First Embodiment

[0012]A semiconductor device according to the present embodiment includes an element region which is a part a semiconductor layer including a first surface and a second surface; a termination region which is a part of the semiconductor layer and surrounds the element region; a first electrode which is provided on the first surface; a second electrode which is provided on the second surface; a first semiconductor region of a first conductive type which is provided in the semiconductor layer and a part of which comes into contact with the first electrode; a second semiconductor region of a second conductive type which is provided between the first semiconductor region in the element region and the first electrode; a third semiconductor region of the second conductive type which is provided between the second semiconductor region and the first electrode, is electrically coupled to the first electrode, and in which impurity concentration of the second conductive type is higher than impurity concentration of the second semiconductor region; and a fourth semiconductor region of the second conductive type which is provided between the first semiconductor region in the termination region and the first surface, is electrically coupled to the first electrode, and in which a distance between the fourth semiconductor region and the second surface is greater than a distance between the second surface and the second semiconductor region.

[0013]A semiconductor device according to the present embodiment includes a semiconductor layer including a first surface and a second surface; a first electrode which is provided on the first surface; a second electrode which is provided on the second surface; a first semiconductor region of a first conductive type which is provided in the semiconductor layer and a part of which comes into contact with the first electrode; a second semiconductor region of a second conductive type which is provided between the first semiconductor region and the first electrode; a third semiconductor region of the second conductive type which is provided in the semiconductor layer between the second semiconductor region and the first electrode, is electrically coupled to the first electrode, and in which impurity concentration of the second conductive type is higher than impurity concentration of the second semiconductor region; and a fourth semiconductor region of the second conductive type which is provided in the semiconductor layer so as to surround the second semiconductor region, is electrically coupled to the first electrode, and in which a distance between the fourth semiconductor region and the second surface is greater than a distance between the second surface and the second semiconductor region.

[0014]FIG. 1 is a schematic sectional view of a semiconductor device according to the present embodiment. FIG. 2 is a schematic top view of the semiconductor device of the present embodiment. FIG. 2 illustrates an impurity region on a first surface side of a semiconductor layer. FIG. 1 corresponds to a cross section taken along line I-I of FIG. 2.

[0015]The semiconductor device according to the present embodiment is a junction barrier Schottky diode (JBS). The JBS 100 according to the present embodiment is a trench type JBS 100 in which a p-type region is provided in a bottom portion of a trench formed in an element region.

[0016]A semiconductor layer of the JBS 100 includes an element region and a termination region. The element region is surrounded by the termination region.

[0017]The element region functions as a region through which a current mainly flows at the time of a forward bias of the JBS 100. The termination region functions as a region which reduces the strength of an electric field that is applied to an end portion of the element region at the time of a reverse bias of the JBS 100 and increases breakdown voltages of elements of the JBS 100.

[0018]The JBS 100 includes a SiC layer (semiconductor layer) 10, an anode electrode (first electrode) 12, a cathode electrode (second electrode) 14, a field oxide film 16, and a silicide layer 30. The SiC layer 10 includes a first surface and a second surface. The anode electrode 12 is provided on the first surface of the SiC layer 10. The cathode electrode 14 is provided on the second surface of the SiC layer 10. The field oxide film 16 is provided on the first surface of the SiC layer 10.

[0019]The SiC layer 10 includes an n+-type cathode region (sixth semiconductor region) 18, an n--type drift region (first semiconductor region) 20, a first anode region of a p-type (second semiconductor region) 22, a second anode region of a p+-type (third semiconductor region) 24, a p--type RESURF region (fourth semiconductor region) 26, a p-type region (fifth semiconductor region) 28, a p-type edge region 23, and a p+-type edge contact region 25.

[0020]The first anode region of a p-type (second semiconductor region) 22, the second anode region of a p+-type (third semiconductor region) 24, and the p-type region (fifth semiconductor region) 28 are provided in the element region. The p--type RESURF region (fourth semiconductor region) 26 is provided in the termination region.

[0021]The SiC layer 10 is SiC (silicon carbide) of single crystal. The SiC layer 10 is, for example, 4H-SiC. A case in which the first surface of the SiC layer 10 is a surface inclined to an angle greater than or equal to zero degrees and smaller than or equal to eight degrees with respect to (0001) surface, and the second surface is a surface inclined to an angle greater than or equal to zero degrees and smaller than or equal to eight degrees with respect to (000-1) surface will be used as an example. The (0001) surface is referred to as a silicon surface. The (000-1) surface is referred to as a carbon surface.

[0022]The n+-type cathode region 18 is provided in the SiC layer 10. The n+-type cathode region 18 is provided between the cathode electrode 14 and the n--type drift region 20.

[0023]The n+-type cathode region 18 contains n-type impurity. The n-type impurity is, for example, nitride (N). Impurity concentration of the n-type impurity is, for example, higher than or equal to 1´1018 cm-3 and lower than or equal to 1´1021 cm-3. Impurity concentration of the n-type impurity of the n+-type cathode region 18 is higher than impurity concentration of the n-type impurity of the n--type drift region 20. A part of the n--type drift region 20 comes into contact with the anode electrode 12.

[0024]The n--type drift region 20 is provided in the SiC layer 10. The n--type drift region 20 is provided on the n+-type cathode region 18.

[0025]The n--type drift region 20 contains n-type impurity. The n-type impurity is, for example, nitride (N). Impurity concentration of the n-type impurity is, for example, higher than or equal to 1´1015 cm-3 and lower than or equal to 2´1016 cm-3. A thickness of the n--type drift region 20 is, for example, greater than or equal to 3 mm and smaller than 30 mm.

[0026]It doesn’t matter that an n-type barrier layer (not illustrated) with impurity concentration of the n-type impurity between the impurity concentration of the n+-type cathode region 18 and the impurity concentration of the n--type drift region 20 is provided between the n+-type cathode region 18 and the n--type drift region 20.

[0027]The first anode region of a p-type 22 is provided in the SiC layer 10. The first anode region of a p-type 22 is provided between the n--type drift region 20 and the anode electrode 12.

[0028]The first anode region of a p-type 22 is provided in a bottom portion of a trench formed on the first surface. For example, after the trench is formed on the first surface, the first anode region of a p-type 22 is formed by injecting p-type impurity into the SiC layer 10, using an ion injection method. A depth of the trench is, for example, greater than or equal to 0.3 mm and smaller than or equal to 1.0 mm.

[0029]The first anode region of a p-type 22 is provided, for example, so as to surround the second anode region of a p+-type 24, as illustrated in FIG. 2.

[0030]The first anode region of a p-type 22 contains p-type impurity. The p-type impurity is, for example, aluminum (Al). Impurity concentration of the p-type impurity is, for example, higher than or equal to 5´1016 cm-3 and lower than or equal to 5´1018 cm-3.

[0031]A depth of the first anode region of a p-type 22 which uses the first surface as a reference is, for example, greater than or equal to 0.7 mm and smaller than or equal to 2.0 mm. A width (“w1” of FIG. 1) of the first anode region of a p-type 22 is, for example, greater than or equal to 5.0 mm and smaller than or equal to 20.0 mm.

[0032]The second anode region of a p+-type 24 is provided in the SiC layer 10. The second anode region of a p+-type 24 is provided between the first anode region of a p-type 22 and the anode electrode 12. The second anode region of a p+-type 24 is provided in the inside of the first anode region of a p-type 22. The second anode region of a p+-type 24 is electrically coupled to the anode electrode 12.

[0033]The second anode region of a p+-type 24 is provided in a bottom portion of a trench formed on the first surface. For example, after the trench is formed on the first surface, the second anode region of a p+-type 24 is formed by injecting p-type impurity into the SiC layer 10 using an ion injection method, by using a mask member having an open part through which a part of the trench is exposed as a mask. A depth of the trench is, for example, greater than or equal to 0.3 mm and smaller than or equal to 1.0 mm.

[0034]The second anode region of a p+-type 24 contains p-type impurity. The p-type impurity is, for example, aluminum (Al). Impurity concentration of the second anode region of a p+-type 24 is higher than impurity concentration of the first anode region of a p-type 22. Impurity concentration of the P-type impurity is, for example, higher than or equal to 1´1019 cm-3 and lower than or equal to 1´1021 cm-3.

[0035]A depth of the second anode region of a p+-type 24 which uses the first surface as a reference is, for example, greater than or equal to 0.5 mm and smaller than or equal to 1.2 mm. A width the second anode region of a p+-type 24 is, for example, greater than or equal to 2.0 mm and smaller than or equal to 15.0 mm.

[0036]The p-type edge region 23 is provided in the SiC layer 10. The p-type edge region 23 is provided between the n--type drift region 20 and the anode electrode 12.

[0037]The p-type edge region 23 is provided in a bottom portion of a trench formed on the first surface. For example, after the trench is formed on the first surface, the p-type edge region 23 is formed by injecting p-type impurity into the SiC layer 10, using an ion injection method. A depth of the trench is, for example, greater than or equal to 0.3 mm and smaller than or equal to 1.0 mm. The p-type edge region 23 is formed at the same time as the first anode region of a p-type 22 by the same process steps as the first anode region of a p-type 22.

[0038]The p-type edge region 23 is provided, for example, in a ring shape in the periphery of an element region as illustrated in FIG. 2.

[0039]The p-type edge region 23 contains p-type impurity. The p-type impurity is, for example, aluminum (Al). Impurity concentration of p-type impurity is, for example, higher than or equal to 5´1016 cm-3 and lower than or equal to 5´1018 cm-3.

[0040]A depth of the p-type edge region 23 which uses the first surface as a reference is, for example, greater than or equal to 0.7 mm and smaller than or equal to 2.0 mm. The depth of the p-type edge region 23 is equal to the depth of the first anode region of a p-type 22.

[0041]The p+-type edge contact region 25 is provided in the SiC layer 10. The p+-type edge contact region 25 is provided between the p-type edge region 23 and the anode electrode 12. The p+-type edge contact region 25 is provided in the inside of the p-type edge region 23. The p+-type edge contact region 25 is electrically coupled to the anode electrode 12. The p+-type edge contact region 25 is provided, for example, in a ring shape in the periphery of an element region as illustrated in FIG. 2.

[0042]The p+-type edge contact region 25 is provided in a bottom portion of a trench formed on the first surface. For example, after the trench is formed on the first surface, 25 is formed by injecting p-type impurity into the SiC layer 10 using an ion injection method, by using a mask member having an open part through which a part of the trench is exposed as a mask. A depth of the trench is, for example, greater than or equal to 0.3 mm and smaller than or equal to 1.0 mm. The p+-type edge contact region 25 is formed, for example, at the same time as the second anode region of a p+-type 24 by the same process steps as the second anode region of a p+-type 24.

[0043]The p+-type edge contact region 25 contains p-type impurity. The p-type impurity is, for example, aluminum (Al). Impurity concentration of the p+-type edge contact region 25 is higher than impurity concentration of the p-type edge region 23. Impurity concentration of the p-type impurity is, for example, higher than or equal to 1´1019 cm-3 and lower than or equal to 1´1021 cm-3.

[0044]A depth of the p+-type edge contact region 25 which uses the first surface as a reference is, for example, greater than or equal to 0.5 mm and smaller than or equal to 1.2 mm.

[0045]The p--type RESURF region 26 is provided in the SiC layer 10. The p--type RESURF region 26 is provided so as to surround the first anode region of a p-type 22 and the p-type region 28. The p--type RESURF region 26 is electrically coupled to the anode electrode 12.

[0046]A distance (“d2” of FIG. 1) between the second surface and the p--type RESURF region 26 is greater than a distance (“d1” of FIG. 1) between the second surface and the first anode region of a p-type 22. That is, d2 > d1. In other words, a depth of the p--type RESURF region 26 which uses the first surface as a reference is smaller than a depth of the first anode region of a p-type 22 which uses the first surface as a reference.

[0047]Since a thickness of the n+-type cathode region 18 is approximately constant, a distance between the n+-type cathode region 18 and the p--type RESURF region 26 is greater than a distance between the n+-type cathode region 18 and the first anode region of a p-type 22. In other words, a thickness of the n--type drift region 20 between the n+-type cathode region 18 and the p--type RESURF region 26 is greater than a thickness of the n--type drift region 20 between the n+-type cathode region 18 and the first anode region of a p-type 22.

[0048]The p--type RESURF region 26 has a termination structure for increasing a breakdown voltage of the JBS 100.

[0049]The p--type RESURF region 26 contains p-type impurity. The p-type impurity is, for example, aluminum (Al). Impurity concentration of the p-type impurity is, for example, higher than or equal to 1´1016 cm-3 and lower than or equal to 1´1018 cm-3.

[0050]Impurity concentration of the p-type impurity of the p--type RESURF region 26 is lower than the impurity concentration of the p-type impurity of the first anode region of a p-type 22 and the p-type edge region 23.

[0051]A plurality of p-type regions 28 are provided in the SiC layer 10 which is surrounded by the p--type RESURF region 26. A width (“w2” of FIG. 1) of the p-type region 28 is smaller than the width (“w1” of FIG. 1) of the first anode region of a p-type 22. That is, w2 < w1. The p-type region 28 comes into contact with the anode electrode 12.

[0052]The p-type region 28 is, for example, a stripe shape, as illustrated in FIG. 2.

[0053]The distance (“d2” of FIG. 1) between the second surface and the p--type RESURF region 26 is greater than a distance (“d3” of FIG. 1) between the second surface and the p-type region 28. That is, d2 > d3. In other words, a depth of the p--type RESURF region 26 which uses the first surface as a reference is smaller than the depth of the p-type region 28 which uses the first surface as a reference.

[0054]The p-type region 28 contains p-type impurity. The p-type impurity is, for example, aluminum (Al). Impurity concentration of the p-type impurity is, for example, higher than or equal to 5´1016 cm-3 and lower than or equal to 5´1018 cm-3.

[0055]A depth of the p-type region 28 which uses the first surface as a reference is, for example, greater than or equal to 0.7 mm and smaller than or equal to 2.0 mm. A width (“w2” of FIG. 1) of the p-type region 28 is, for example, greater than or equal to 1.0 mm and smaller than or equal to 3.0 mm. An interval between the p-type regionss 28 is, for example, greater than or equal to 1.0 mm and smaller than or equal to 5.0 mm.

[0056]The p-type region 28 is provided in a bottom portion of a trench formed on the first surface. For example, after the trench is formed on the first surface, the p-type region 28 is formed by injecting p-type impurity into the SiC layer 10, using an ion injection method. A depth of the trench is, for example, greater than or equal to 0.3 mm and smaller than or equal to 1.0 mm.

[0057]For example, the distance (“d1” of FIG. 1) between the second surface and the first anode region of a p-type 22 is approximately equal to a distance (“d3” of FIG. 1) between the second surface and the p-type region 28. That is, d1 = d3. In addition, impurity concentration of the p-type impurity of the first anode region of a p-type 22 is approximately equal to impurity concentration of the p-type impurity of the p-type region 28.

[0058]For example, the p-type region 28 and the first anode region of a p-type 22 are formed by the same process steps. For example, a trench for forming the p-type region 28 and a trench for forming the first anode region of a p-type 22 are simultaneously formed. Thereafter, the p-type impurity is injected into a bottom portion of the trench using an ion injection method, and the impurity is activated by activation annealing.

[0059]By the process steps, the distance (“d1” of FIG. 1) between the second surface and the first anode region of a p-type 22 becomes approximately equal to the distance (“d3” of FIG. 1) between the second surface and the p-type region 28. In addition, the impurity concentration of the p-type impurity of the first anode region of a p-type 22 becomes approximately equal to the impurity concentration of the p-type impurity of the p-type region 28.

[0060]The silicide layer 30 is provided between the second anode region of a p+-type 24 and the anode electrode 12. The silicide layer 30 is, for example, a nickel silicide layer or a titanium silicide layer. A thickness of the n--type drift region 20 is, for example, greater than or equal to 0.05 mm and smaller than or equal to 0.3 mm.

[0061]The field oxide film 16 is provided on the p--type RESURF region 26. The field oxide film 16 is, for example, a silicon oxide film. The field oxide film 16 includes an opening. A thickness of the field oxide film 16 is, for example, greater than or equal to 0.2 mm and smaller than or equal to 1.0 mm.

[0062]The anode electrode 12 comes into contact with the n--type drift region 20, the silicide layer 30, and the p-type region 28 through an opening of the field oxide film 16. The trench provided on the first anode region of a p-type 22 and the trench provided on the p-type region 28 are buried in the anode electrode 12. In other words, a part of the anode electrode 12 on the first anode region of a p-type 22 is interposed in the n--type drift region 20. In addition, a part of the anode electrode 12 on the p-type region 28 is interposed in the n--type drift region 20.

[0063]The anode electrode 12 comes into contact with the n--type drift region 20, an upper portion of the first surface, and a side surface of the trench. Contact between the n--type drift region 20 and the anode electrode 12 is Schottky contact.

[0064]The anode electrode 12 is a metal. The anode electrode 12 is, for example, a stacked film of titanium (Ti) and aluminum (Al).

[0065]The cathode electrode 14 is provided so as to come into contact with the n+-type cathode region 18. Contact between the cathode electrode 14 and the n+-type cathode region 18 is Ohmic contact.

[0066]The cathode electrode 14 is a metal. The cathode electrode 14 is, for example, a stacked film of titanium (Ti) and aluminum (Al).

[0067]Next, actions and effects of the JBS 100 will be described.

[0068]FIG. 3 is a schematic sectional view of a semiconductor device according to a comparative form. The semiconductor device according to the comparative form is a JBS. A JBS 900 according to the comparative form is a planar type JBS without a trench in a different manner from the JBS 100 according to the present embodiment.

[0069]In the JBS 900, the first anode region of a p-type 22 and the p-type region 28 are provided in a first surface, not in a bottom portion of a trench. The distance (“d2” of FIG. 3) between a second surface and the p--type RESURF region 26 is smaller than the distance (“d1” of FIG. 3) between the second surface and the first anode region of a p-type 22. That is, d2 < d1.

[0070]In addition, the distance (“d2” of FIG. 3) between the second surface and the p--type RESURF region 26 is smaller than a distance (“d3” of FIG. 3) between the second surface and the p-type region 28. That is, d2 < d3.

[0071]The JBS 900 includes an n-type region 32 between the n--type drift region 20 and the first anode region of a p-type 22. The n-type region 32 contains n-type impurity. The n-type impurity is, for example, nitride (N). Impurity concentration of the n-type impurity is, for example, higher than or equal to 1´1017 cm-3 and lower than or equal to 1´1019 cm-3. Impurity concentration of the n-type impurity of the n-type region 32 is higher than impurity concentration of the n-type impurity of the n--type drift region 20.

[0072]In the JBS 900, by providing the p-type region 28, the n--type drift region 20 between the p-type regions 28 is pinched off by depletion layers, if a reverse bias is applied to the JBS 900. Hence, it is possible to reduce a reverse current (IR) of the JBS 900.

[0073]Furthermore, the JBS 900 includes the anode electrode 12, the silicide layer 30, the second anode region of a p+-type 24, the first anode region of a p-type 22, the n-type region 32, the n--type drift region 20, and a PiN diode section configured by the cathode electrode 14, in an element region. By including the PiN diode section, it is possible to make a large forward surge current flow.

[0074]In addition, in the JBS 900, by providing the n-type region 32 in the PiN diode section, the profile of a pn junction is steepened, and a junction breakdown voltage of the PiN diode section is lower than a junction breakdown voltage of a termination structure formed by the p--type RESURF region 26.

[0075]Hence, junction breakdown at the time of a reverse bias is easily made by the PiN diode section rather than a termination structure. In the PiN diode section, the junction breakdown is made in a wider area than the termination structure. For this reason, it is possible to prevent heat or the like from being generated due to the junction breakdown, and to prevent an element from being broken down.

[0076]Furthermore, in the JBS 900, the junction breakdown voltage of the PiN diode section is lower than the junction breakdown voltage of the termination structure formed in the p--type RESURF region 26, and thus an additional process step for forming the n-type region 32 is needed. In addition, by providing the n-type region 32, there is possibility that a junction leakage current of the PiN diode section at the time of a reverse bias increases due to crystal defects or the like, and a reverse current (IR) of the JBS 900 increases.

[0077]In addition, in the JBS 900, the p-type region 28 or the first anode region of a p-type 22 is provided in an element region. For this reason, a contact area between the anode electrode 12 and the n--type drift region 20, that is, an area of Schottky contact decreases, and a forward voltage (VF) of the JBS 900 increases.

[0078]In the JBS 100 according to the present embodiment, the distance (“d2” of FIG. 1) between the second surface and the p--type RESURF region 26 is greater than the distance (“d1” of FIG. 1) between the second surface and the first anode region of a p-type 22. That is, d2 > d1.

[0079]Hence, the thickness of the n--type drift region 20 under the PiN diode section becomes smaller than that of the JBS 900. The junction breakdown voltage of the PiN diode section decreases as the thickness of the n--type drift region 20 is shallowed. Hence, in the JBS 100 according to the present embodiment, it is possible to decrease the junction breakdown voltage of the PiN diode section without providing the n-type region 32.

[0080]Particularly, since the thickness of the n--type drift region 20 under the PiN diode section is smaller than the thickness of the n--type drift region 20 under the RESURF region 26, the junction breakdown at the time of a reverse bias is easily made by the PiN diode section rather than the termination structure.

[0081]In addition, since the n-type region 32 is not provided, it is possible to more reduce the reverse current (IR) than the JBS 900.

[0082]Furthermore, by providing a trench type JBS, a forward voltage (VF) can be reduced. Reduction of the forward voltage (VF) can be realized by making the anode electrode 12 come into contact with the n--type drift region 20 from a viewpoint of the trench, and increasing an area of Schottky contact.

[0083]In the JBS 100, it is possible to improve trade-off between the forward voltage (VF) and the reverse voltage (IR) by providing the trench type JBS.

[0084]In addition, according to the JBS 100 according to the present embodiment, it is possible to easily form a trench type JBS and a PiN diode section with a low junction breakdown voltage, using the same process steps. Particularly, it is hard to form a deep impurity region in the SiC layer, using an ion injection method, compared to, for example, a silicon (Si) layer. Hence, process steps in which the deep first anode region of a p-type 22 can be formed by using trench formation of the trench type JBS is valid.

[0085]It is preferable that impurity concentration of the p-type impurity of the p--type RESURF region 26 is lower than impurity concentration of the p-type impurity of the first anode region of a p-type 22, from a viewpoint in which junction breakdown at the time of a reverse bias is easily made in a PiN diode section rather than in a termination structure.

[0086]In addition, it is preferable that the silicide layer 30 is provided from a viewpoint in which a resistance between the anode electrode 12 and the first anode region of a p-type 22 is reduced.

[0087]As such, according to the present embodiment, it is possible to realize the JBS 100 which can prevent an element from being broken down at the time of a reverse bias. In addition, it is possible to realize the JBS 100 in which a reverse current (IR) is reduced. In addition, it is possible to realize the JBS 100 in which a forward voltage (VF) is reduced.

Second Embodiment

[0088]A semiconductor device according to the present embodiment is the same as the semiconductor device according to the first embodiment except that the semiconductor device according to the present embodiment does not include the fifth semiconductor region. Hence, description of the contents which overlap the contents of the first embodiment will be omitted.

[0089]FIG. 4 is a schematic sectional view of a semiconductor device according to the present embodiment.

[0090]The semiconductor device according to the present embodiment is an SBD. The SBD 200 according to the present embodiment is different from the JBS 100 according to the first embodiment, and does not include the p-type region 28.

[0091]The SBD 200 includes an element region and a termination region. The element region is surrounded by the termination region.

[0092]The SBD 200 includes the SiC layer (semiconductor layer) 10, the anode electrode (first electrode) 12, the cathode electrode (second electrode) 14, the field oxide film 16, and the silicide layer 30. The SiC layer 10 includes the first surface and the second surface. The anode electrode 12 is provided on the first surface of the SiC layer 10. The cathode electrode 14 is provided on the second surface of the SiC layer 10. The field oxide film 16 is provided on the first surface of the semiconductor layer 10.

[0093]The SiC layer 10 includes the n+-type cathode region (sixth semiconductor region) 18, the n--type drift region (first semiconductor region) 20, the first anode region of a p-type (second semiconductor region) 22, the second anode region of a p+-type (third semiconductor region) 24, the p--type RESURF region (fourth semiconductor region) 26, the p-type edge region 23, and the p+-type edge contact region 25.

[0094]The first anode region of a p-type 22 is provided in a bottom portion of the trench formed on the first surface. For example, after the trench is formed on the first surface, the first anode region of a p-type 22 is formed by injecting p-type impurity into the SiC layer 10, using an ion injection method.

[0095]A distance (“d2” of FIG. 4) between the second surface and the p--type RESURF region 26 is greater than a distance (“d1” of FIG. 4) between the second surface and the first anode region of a p-type 22. That is, d2 > d1. In other words, a depth of the p--type RESURF region 26 which uses the first surface as a reference is smaller than a depth of the first anode region of a p-type 22 which uses the first surface as a reference.

[0096]According to the present embodiment, it is possible to realize the SBD 200 which can prevent an element from being broken down at the time of a reverse bias, using the same actions as the first embodiment.

[0097]In the first and second embodiments, an example in which a SiC layer is used as a semiconductor layer is described, but exemplary embodiments can also be applied to a diode which uses, for example, a silicon (Si) layer in addition to the SiC layer.

[0098]In addition, in the first and second embodiments, a case in which 4H-SiC is used as SiC is used as an example, but other crystal forms such as 3C-SiC or 6H-SiC can also be used.

[0099]In addition, in the first and second embodiments, a case in which, if the semiconductor layer is the SiC layer, the first surface is a surface inclined to an angle greater than or equal to zero degrees and smaller than or equal to eight degrees with respect to (0001) surface, and the second surface is a surface inclined to an angle greater than or equal to zero degrees and smaller than or equal to eight degrees with respect to (000-1) surface is used as an example, but other surfaces of surface orientation can also be used.

[0100]In addition, in the first and second embodiments, an example in which nitride is used as n-type impurity is described, but phosphorus (P), arsenic (As), antimony (Sb), or the like can also be applied. In addition, an example in which aluminum (Al) is used as p-type impurity is described, but boron (B) can also be used.

[0101]In addition, in the first and second embodiments, an example in which an n-type is used as the first conductive type and a p-type is used as the second conductive type is described, but a p-type can also be used as the first conductive type and an n-type can also be used as the second conductive type.

[0102]In addition, in the first embodiment, a case in which Schottky contact of the anode electrode 12 is provided on a side surface of a trench, but a form in which the side surface of the trench is covered with the p-type region 28 can also be used.

[0103]In addition, in the first embodiment, an example in which a trench type JBS is used is described, but exemplary embodiments can also be applied to a planar type JBS in which the p-type region 28 is provided on the first surface.

[0104]In addition, the shape of the first anode region 22 is not limited to the shape of FIG. 2, and can be formed by other shapes such as a stripe shape or a dot shape. In addition, the shape of the p-type region 28 is not limited to the shape of FIG. 2, and can be formed by other shapes such as a ring shape or a dot shape.

[0105]In addition, in the first and second embodiments, a case in which the trench is provided on the first anode region 22 is described as an example, but a form in which the first anode region22 is provided on the first surface without providing the trench can also be used. If this case is used, the first anode region 22 is formed by, for example, high speed ion injection of p-type impurity.

[0106]While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

an element region which is a part a semiconductor layer including a first surface and a second surface;

a termination region which is a part of the semiconductor layer and surrounds the element region;

a first electrode which is provided on the first surface;

a second electrode which is provided on the second surface;

a first semiconductor region of a first conductive type which is provided in the semiconductor layer and a part of which comes into contact with the first electrode;

a second semiconductor region of a second conductive type which is provided between the first semiconductor region in the element region and the first electrode;

a third semiconductor region of the second conductive type which is provided between the second semiconductor region and the first electrode, is electrically coupled to the first electrode, and in which impurity concentration of the second conductive type is higher than impurity concentration of the second semiconductor region; and

a fourth semiconductor region of the second conductive type which is provided between the first semiconductor region in the termination region and the first surface, is electrically coupled to the first electrode, and in which a distance between the fourth semiconductor region and the second surface is greater than a distance between the second surface and the second semiconductor region.

2. The device according to Claim 1, wherein impurity concentration of the second conductive type of the fourth semiconductor region is lower than impurity concentration of the second conductive type of the second semiconductor region.

3. The device according to Claim 1 or 2, further comprising:

a plurality of fifth semiconductor regions of the second conductive type, each being provided in the element region, being electrically coupled to the first electrode, and having a width smaller than a width of the second semiconductor region.

4. The device according to Claim 3, wherein a distance between the second surface and the fourth semiconductor region is greater than a distance between the second surface and the fifth semiconductor region.

5. The device according to Claim 3 or 4, wherein a distance between the second surface and the second semiconductor region is approximately equal to a distance between the second surface and the fifth semiconductor region, and impurity concentration of the second conductive type of the second semiconductor region is approximately equal to impurity concentration of the second conductive type of the fifth semiconductor region.

6. The device according to any one of Claims 3 to 5, wherein the fifth semiconductor region comes into contact with the first electrode.

7. The device according to any one of Claims 1 to 6, wherein a part of the first electrode on the second semiconductor region is interposed between the first semiconductor regions.

8. The device according to any one of Claims 1 to 7, wherein a part of the first electrode on the fifth semiconductor region is interposed between the first semiconductor regions.

9. The device according to any one of Claims 1 to 8, further comprising:

a sixth semiconductor regions of the first conductive type which is provided between the second electrode and the first semiconductor region, and in which impurity concentration of the first conductive type is higher than impurity concentration of the first semiconductor region.

10. The device according to any one of Claims 1 to 9, wherein contact between the first semiconductor region and the first electrode is Schottky contact.

11. The device according to any one of Claims 1 to 10, wherein the semiconductor layer is a SiC layer.

12. The device according to any one of Claims 1 to 11, further comprising:

a silicide layer which is provided between the third semiconductor region and the first electrode.

13. A semiconductor device comprising:

an element region which is a part a semiconductor layer including a first surface and a second surface;

a termination region which is a part of the semiconductor layer and surrounds the element region;

a first electrode which is provided on the first surface;

a second electrode which is provided on the second surface;

a first semiconductor region of a first conductive type which is provided in the semiconductor layer and a part of which comes into contact with the first electrode;

a second semiconductor region of a second conductive type which is provided between the first semiconductor region in the element region and the first electrode;

a third semiconductor region of the second conductive type which is provided between the second semiconductor region and the first electrode, is electrically coupled to the first electrode, and in which impurity concentration of the second conductive type is higher than impurity concentration of the second semiconductor region; and

a fourth semiconductor region of the second conductive type which is provided between the first semiconductor region in the termination region and the first surface, is electrically coupled to the first electrode, and whose depth that uses the first surface as a reference is smaller than a depth of the second semiconductor region that uses the first surface as a reference.

ABSTRACT

According to one embodiment, a semiconductor device includes an element region which is a part a semiconductor layer including a first surface and a second surface; a termination region which surrounds the element region; a first electrode which is provided on the first surface; a second electrode which is provided on the second surface; a first semiconductor region of a first conductive type which is provided in the semiconductor layer and a part of which comes into contact with the first electrode; a second semiconductor region of a second conductive type which is provided between the first semiconductor region in the element region and the first electrode; a third semiconductor region of the second conductive type which is provided between the second semiconductor region and the first electrode, is electrically coupled to the first electrode, and in which impurity concentration of the second conductive type is higher than impurity concentration of the second semiconductor region; and a fourth semiconductor region of the second conductive type which is provided between the first semiconductor region in the termination region and the first surface, is electrically coupled to the first electrode, and in which a distance between the fourth semiconductor region and the second surface is greater than a distance between the second surface and the second semiconductor region.

DRAWINGS

FIG. 1

TERMINATION REGION

ELEMENT REGION

TERMINATION REGION

FIRST SURFACE

SECOND SURFACE

FIG. 3

TERMINATION REGION

ELEMENT REGION

TERMINATION REGION

FIRST SURFACE

SECOND SURFACE

FIG. 4

TERMINATION REGION

ELEMENT REGION

TERMINATION REGION

FIRST SURFACE

SECOND SURFACE